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[Abstract of the Disclosure]

[Abstract]

5 The present invention provides a semiconductor device that is able to suppress a leakage current and a method of forming the same. The semiconductor device includes an ohmic layer and a pad contact plug that are sequentially stacked through an interlayer dielectric under a capacitor. The ohmic layer is electrically connected to a part of a resistor at the
10 peripheral circuit region. The pad contact plug is disposed to be lower than a metal contact plug. The ohmic layer may be formed before formation of the capacitor. Thus, elements in the cell array region are not degraded even if a metal contact plug is formed in a peripheral circuit region after elements such as a capacitor are formed in a cell array region in a subsequent process.

15 [Typical Figure]

FIG. 1

[Index]

20 ohmic layer, capacitor, metal contact

[Specification]

[Title of the Invention]

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**SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE
SAME**

[Brief Description of the Drawings]

10 Fig. 1 is a cross-sectional view showing several steps of a
conventional method for fabricating a semiconductor device.

 Fig. 2 is a cross-sectional view of a semiconductor device according
to the present invention.

 Fig. 3 through Fig. 10 are cross-sectional views of a method of
15 fabricating a semiconductor device according to the present invention.

[Detailed Description of the Invention]

[Object of the Invention]

20

[Field of the Invention and Prior Art related to the Invention]

 The present invention relates to semiconductor devices and methods
of forming the same. More particularly, the present invention relates to

semiconductor devices having resistors and methods of forming the same.

In a semiconductor device, a resistor is typically made of polysilicon doped with impurities because resistance of the resistor is readily controlled by changing doping concentration of impurities.

5 Fig. 1 is a cross-sectional view showing several steps of a conventional method for fabricating a semiconductor device.

Referring to Fig. 1, a lower interlayer dielectric 3 is stacked on a semiconductor substrate 1. At a cell array region A, the lower interlayer dielectric 3 is patterned to form a contact hole exposing the semiconductor
10 substrate 1 and the contact hole is filled with a conductive material to form a buried contact plug 5. A first etch stopping layer 7 and a first interlayer dielectric 9 are sequentially stacked on the buried contact plug 5 and the lower interlayer dielectric 3. At the cell array region A, the first interlayer dielectric 9 and the first etch stopping layer 7 are sequentially patterned to
15 form a pad contact hole exposing the buried contact plug 5. At this time, at a peripheral circuit region B, all of the first interlayer dielectric 9 may be patterned to be removed. The pad contact hole is filled with a conductive material to form a pad contact plug 11. At the peripheral circuit region B, all of the conductive material is removed to expose the lower interlayer
20 dielectric 3. A doped polysilicon layer is formed at an entire surface of the semiconductor substrate 1 and patterned to form a resistor 15 at the peripheral circuit region B. At this time, at the cell array region A, all of the doped polysilicon layer is removed to expose the first interlayer dielectric 9

and the pad contact plug 11. A second etch stopping layer 17 is formed at an entire surface of the semiconductor substrate 1 having the resistor 15. A bottom electrode 18 is formed to electrically connect to the pad contact plug 11 through the second etch stopping layer 17. A dielectric layer 19 and an upper electrode 21 is conformally formed along a profile of the bottom electrode 18 to compose a capacitor. At the peripheral circuit region B, the upper electrode 21 is entirely removed by means of a patterning process. A second interlayer dielectric 23 is stacked to cover the capacitor and the second etch stopping layer 17. At the peripheral circuit region B, the second interlayer dielectric 23 and the second etch stopping layer 17 are sequentially patterned to form a metal contact hole 24 exposing a part of the resistor 15. Before forming a metal contact plug of a metal in the metal contact hole 24, an ohmic layer 26 is required in order to reduce resistance difference between the metal of the metal contact plug and the polysilicon of the resistor 15. In order to form the ohmic layer 26, a metal layer 26 such as titanium is conformally stacked and a rapid thermal process is performed at a temperature higher than 600°C. At this time, the polysilicon of the resistor 15 reacts with the metal layer 25 of titanium to form the ohmic layer 26 of metal silicide such as titanium silicide. However, at the cell array region A, during the rapid thermal process at the temperature higher than 600°C, the dielectric layer 19 of the capacitor is damaged to increase a leakage current when a semiconductor device is operated.

Therefore, in a case where a device such as a capacitor is formed at a

cell array region after forming a resistor of a polysilicon at a peripheral circuit region, the device such as the capacitor may be damaged in the thermal process of forming an ohmic layer at a temperature higher than 600°C. Thus, reliability of semiconductor devices is degraded.

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[Technical Object of the Invention]

It is therefore an object of the present invention to provide semiconductor devices that is able to suppress a leakage current and improve a reliability of the semiconductor device.

10

It is another object of the present invention to provide methods of forming semiconductor devices that is able to suppress a leakage current and improve a reliability of the semiconductor device.

[Construction of the Invention]

15

In order to achieve these objects, the present invention provides semiconductor devices including an ohmic layer and a pad contact plug that are sequentially stacked. The ohmic layer is electrically connected to a part of a resistor at the peripheral circuit region. The pad contact plug has a height lower than a metal contact plug.

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More specifically, the semiconductor device includes a semiconductor substrate having a cell array region and a peripheral circuit region; a lower interlayer dielectric covering the semiconductor substrate; a buried contact plug electrically connecting to the semiconductor substrate

through the lower interlayer dielectric at the cell array region; a resistor on the lower at the peripheral circuit region; a first interlayer dielectric covering the buried contact plug, the resistor, the lower interlayer dielectric; a first pad contact plug electrically connecting to the buried contact plug
5 through the first interlayer dielectric at the cell array region; a second pad contact plug electrically connecting to the resistor through the first interlayer dielectric at the peripheral circuit region; an ohmic layer interposed between the first pad contact plug and the buried contact plug and between the second pad contact plug and the resistor; a capacitor having an upper electrode, a
10 dielectric layer, and a bottom electrode electrically connecting to the first pad contact plug at the cell array region; a second interlayer dielectric covering the capacitor and the first interlayer dielectric; and a metal contact plug electrically connecting to the second pad contact plug through the first interlayer dielectric at the peripheral circuit region.

15 The semiconductor device may further include a first adhesion layer interposed between the first pad contact plug and the first interlayer dielectric, between the first pad contact plug and the buried contact plug, between the second pad contact plug and the first interlayer dielectric, and between the second pad contact plug and the resistor; and a second adhesion
20 layer interposed between the metal contact plug and the first interlayer dielectric and between the metal contact plug and the pad contact plug.

An etch stopping layer may be interposed between the first interlayer dielectric and the second interlayer dielectric. The buried contact plug and

the resistor may be of a doped polysilicon. The ohmic layer may be of one selected from the group consisting of titanium silicide (TiSi_x), tantalum silicide (TaSi_y), cobalt silicide (CoSi_z) and nickel silicide (NiSi_w). The first adhesion layer and the second adhesion layer may be of titanium nitride. The first pad contact plug, the second pad contact plug and the metal contact plug may be of one selected from the group consisting of tungsten, aluminum, and copper.

The present invention is provided by a method of forming the semiconductor device. In the method, an ohmic layer electrically connecting to a part of a resistor and a pad contact plug having a height lower than a metal contact plug are formed at a peripheral circuit region before forming a capacitor at a cell array region.

More specifically, the semiconductor device is formed by the following method. First, a cell array region and a peripheral circuit region are defined at a semiconductor substrate. A lower interlayer dielectric is stacked at the semiconductor substrate. A contact hole is formed to expose the semiconductor substrate at the cell array region by patterning the lower interlayer dielectric. The contact hole is filled by stacking a first conductive layer at an entire surface of the semiconductor substrate having the contact hole. The first conductive layer is patterned to form a buried contact plug filling the contact hole at the cell array region and simultaneously to form a resistor on the lower interlayer dielectric at the peripheral circuit region. A first interlayer dielectric is formed to cover the semiconductor substrate

having the buried contact plug and the resistor. The first interlayer dielectric is patterned to form a first pad contact hole exposing the buried contact plug and simultaneously to form a second pad contact hole exposing a part of the resistor. An ohmic layer is formed to cover at least bottoms of the first pad contact hole and the second pad contact hole. The first pad contact hole and the second pad contact hole are filled by stacking a second conductive layer. The second conductive layer is planarized to expose the first interlayer dielectric and to form a first pad contact plug in the first pad contact hole and a second pad contact plug in the second pad contact hole. An etch stopping layer is formed to cover the first pad contact plug, the second pad contact plug and the first interlayer dielectric. A capacitor having an upper electrode, a dielectric layer and a bottom electrode electrically connecting to the first pad contact plug through the etch stopping layer is formed. A second interlayer dielectric is formed at an entire surface of the semiconductor substrate. A metal contact hole is formed to expose the second pad contact plug by patterning the second interlayer dielectric at the peripheral circuit region. A metal contact plug is formed by filling the metal contact hole with a third conductive layer.

In the method, an etch stopping layer may be formed before forming the second interlayer dielectric. The first conductive layer is preferably formed of a doped polysilicon.

In the method, the ohmic layer may be formed by the following sequences. First, a metal layer is formed to cover at least bottoms of the first

pad contact hole and the second pad contact hole. Then, a rapid thermal process is performed with respect to the metal layer to form an ohmic layer at boundaries between the metal layer and the buried contact plug and between the metal layer and the resistor. At this time, the rapid thermal
5 process may be performed at a temperature of about 600~900°C for about 10~30 seconds. The ohmic layer may be preferably formed of one selected from the group consisting of titanium silicide (TiSi_x), tantalum silicide (TaSi_y), cobalt silicide (CoSi_z) and nickel silicide (NiSi_w).

In the method, a first adhesion layer may be formed to cover
10 sidewalls and bottoms of the first pad contact hole and the second pad contact hole before forming the second conductive layer. Additionally, a second adhesion layer may be formed to cover sidewalls and a bottom of the metal contact hole before forming the third conductive layer. At this time, the first adhesion layer and the second adhesion layer are preferably formed
15 of titanium nitride. The second conductive layer and the third conductive layer are preferably formed of one selected from the group consisting of tungsten, aluminum, and copper.

According to the semiconductor device and the method of forming the semiconductor device of the present invention, since an ohmic layer is
20 formed before forming a capacitor, it is possible to prevent leakage current of the capacitor that may occur at the high temperature. Additionally, since the resistor at the peripheral circuit region and the buried contact plug at the cell array region are made of the same material, it is possible to simplify the

total process.

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

In the drawings, the thickness of layers and regions are exaggerated for clarity. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

Furthermore, relative terms, such as "beneath", may be used herein to describe one element's relationship to another elements as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in the Figures is turned over, elements described as "below" other elements would then be oriented "above" the other elements. The exemplary term "below", can therefore, encompass both an orientation of above and below.

It will be understood that although the terms first and second are used herein to describe various regions, layers and/or sections, these regions, layers and/or sections should not be limited by these terms. These terms are

only used to distinguish one region, layer or section from another region, layer or section. Thus, a first region, layer or section discussed below could be termed a second region, layer or section, and similarly, a second without departing from the teachings of the present invention. Like numbers refer to
5 like elements throughout. A reference letter 'A' indicates a cell array region and another reference letter 'B' indicates a peripheral circuit region.

Fig. 2 is a cross-sectional view of a semiconductor device according to the present invention.

Referring to Fig. 2, a lower interlayer dielectric 102 is disposed on a
10 semiconductor substrate 100 having the cell array region A and the peripheral circuit region B. A contact hole 104 exposes the semiconductor substrate 100 through the lower interlayer dielectric 102 at the cell array region A. A buried contact plug 106a fills the contact hole 104 and electrically connects to the semiconductor substrate 100. The buried contact
15 plug 106a may remain only in the contact hole 104 or may cover even a part of the lower interlayer dielectric 102 by being protruded to the outside of the contact hole 104. A resistor is disposed on the lower interlayer dielectric 102 at the peripheral circuit region B. The resistor 108 and the buried contact plug 106a may be formed of the same material, and preferably of a doped
20 polysilicon. A first etch stopping layer 110 conformally covers the resistor 108, the buried contact plug 106a and the lower interlayer dielectric 102. A first interlayer dielectric 112 covers the first etch stopping layer 110. A first pad contact hole 113a exposes the buried contact plug 106a through the first

interlayer dielectric 112 and the first etch stopping layer 110 at the cell array region A. A second pad contact hole 113b exposes the resistor 108 through the first interlayer dielectric 112 and the first etch stopping layer 110 at the peripheral circuit region A. Sidewalls of the first and second pad contact holes 113a and 113b are covered by a metal layer 114, and bottoms of thereof are covered by an ohmic layer 115. The metal layer 114 and the ohmic layer 115 may be covered by a first adhesion layer 116. The metal layer 114 is preferably of one metal selected from the group consisting of titanium, tantalum, cobalt and nickel, and the ohmic layer 115 may be of a silicide of the metal. The first and second pad contact holes 113 and 113b are filled with first and second pad contact plugs 118a and 118b, respectively. The first interlayer dielectric 112 and the first and second pad contact plugs 118a and 118b are covered by a second etch stopping layer 120. The first and second etch stopping layers 110 and 120 may be of silicon nitride. Although not shown, a wet-etch stopping layer may be added to cover the second etch stopping layer 120. A bottom electrode 128a having a cylinder shape electrically connects to the first pad contact plug 118a through the second etch stopping layer 120 at the cell array region A. A dielectric layer 130 and an upper electrode 132 conformally covering a profile of the bottom electrode 128a compose a capacitor at the cell array region A. The bottom electrode 128a and the upper electrode 132 may be of titanium nitride. The dielectric layer 130 may be of hafnium oxide. The upper electrode 132 may be covered by a capping layer of tungsten. A second interlayer dielectric 134

covers the capacitor at the cell array region A and the second etch stopping layer 120 at the peripheral circuit region B. A metal contact hole 136 exposes the second pad contact plug 118b through the second interlayer dielectric 134 and the second etch stopping layer 120 at the peripheral circuit region B. Sidewalls and a bottom of the metal contact hole 136 are covered by a second adhesion layer 138. The first and second adhesion layers 116 and 138 are preferably of titanium nitride. The metal contact hole 136 is filled with a metal contact plug 140. The first and second pad contact plugs 118a and 118b, and the metal contact plug 140 may be of one conductive material selected from a group consisting of tungsten, aluminum, and copper.

In the above structure of the semiconductor device, since the ohmic layer 115 and the pad contact plugs 118a and 118b are disposed in the pad contact holes 113a and 113b penetrating the first interlayer dielectric 112 under the capacitor, the ohmic layer 115 can be formed at a temperature higher than 600°C before forming the capacitor. Thus, it is possible to prevent leakage current and degrading of reliability in a semiconductor device.

Fig. 3 through Fig. 10 are cross-sectional views of a method of fabricating a semiconductor device according to the present invention.

Referring to Fig. 3, a semiconductor substrate 100 is divided into the cell array region A and the peripheral circuit region B. A lower interlayer dielectric 102 is formed on the semiconductor substrate 100. The lower

interlayer dielectric 102 may be formed of a material such as silicon oxide. Although not illustrated in the figures, field oxides and transistors having gate patterns and impurity-doped regions may be formed at the semiconductor substrate 100 before forming the lower interlayer dielectric 102. At the cell array region A, the lower interlayer dielectric 102 is patterned to form a contact hole 104 exposing the semiconductor substrate 100.

Referring to Figs. 4 and 5, a first conductive layer is conformally stacked on an entire surface of the semiconductor substrate 100 having the contact hole 104, thereby filling the contact hole 104. The first conductive layer is patterned to form a buried contact plug 106a or 106b filling the contact hole 104 at the cell array region A and simultaneously to form a resistor 108 covering a part of the lower interlayer dielectric 102 at the peripheral circuit region B. At this time, the buried contact plug may remain only in the contact hole 104 like the reference number 106b in Fig. 5 or may cover a part of the lower interlayer dielectric 102 by being protruded out of the contact hole like the reference number 106a in Fig. 4. The first conductive layer may be formed of a doped polysilicon with a thickness of about 1500Å. At this time, the resistance of the resistor 108 may be controlled by changing the doping concentration of the impurities.

Figs. 6 through 10 are illustrated after Fig. 4.

Referring to Fig. 6, a first etch stopping layer 110 is conformally stacked at an entire surface of the semiconductor substrate 100 having the

resistor 108 and the buried contact plug 106a of Fig. 4. The first etch
stopping layer 110 is preferably formed of silicon nitride with a thickness of
about 150Å. A first interlayer dielectric 112 is stacked on the first etch
stopping layer 100 and planarized. At this time, the first interlayer dielectric
5 112 is preferably formed of high density plasma (HDP) oxide with a
thickness of about 2000Å.

Referring to Fig. 7, the first interlayer dielectric 112 and the first etch
stopping layer 110 are sequentially patterned to form a first pad contact hole
113a exposing the buried contact plug 104 at the cell array region A and
10 simultaneously to form a second pad contact hole 113b exposing the resistor
108 at the peripheral circuit region B. A metal layer 114 is conformally
formed with a thickness of about 85Å at an entire surface of the
semiconductor substrate 100 having the first and second pad contact holes
113a and 113b. The metal layer 114 may be formed of a metal selected from
15 the group consisting of titanium (Ti), tantalum (Ta), cobalt (Co) and nickel
(Ni). A rapid thermal process is performed with respect to the metal layer
114 at a temperature of about 650°C for about 15 seconds, thereby forming
an ohmic layer 115 of metal silicide at boundaries between the metal layer
114 and the buried contact plug 106a and between the metal layer 114 and
20 the resistor 108. The metal layer 114 may be formed by a method such as
sputtering, physical vapor deposition (PVD) or chemical vapor deposition
(CVD). In the case that the metal layer 114 is formed by the CVD method,
the deposition temperature may be 650°C and the metal layer 114 and the

ohmic layer 115 may be simultaneously formed at the boundaries without the rapid thermal process. A first adhesion layer 116 is formed preferably of titanium nitride with a thickness of about 250Å on the ohmic layer 115 and the metal layer 114. A second conductive layer is deposited with a thickness of 2000Å to fill the first and second pad contact holes 113a and 113b. A planarization process is performed with respect to the second conductive layer, the first adhesion layer 116 and the metal layer 114, thereby exposing the first interlayer dielectric 112 and simultaneously forming first and second pad contact plugs 118a and 118b in the first and second pad contact plugs, respectively. The second conductive layer may be formed of a conductive material selected from the group consisting of tungsten, copper, and aluminum.

Referring to Fig. 8, a second etch stopping layer 120 and a mold layer 124 are sequentially formed at an entire surface of the semiconductor substrate having the first and second pad contact plugs 118a and 118b. The second etch stopping layer 120 is preferably formed of silicon nitride with a thickness of about 500Å. Although not illustrated, a wet-etch stopping layer may be formed of tantalum oxide with a thickness of about 90Å on the second etch stopping layer 120. The wet-etch stopping layer may function as an etch stopper when the mold layer 124 is removed by a wet-etch process. The mold layer 124 is made of single layer of boron phosphorus silicate glass (BPSG) or plasma-enhanced tetraethyl orthosilicate (PETEOS, $\text{Si}(\text{OC}_2\text{H}_5)_4$) or dual layer of the BPSG and the PETEOS. In the case that the

mold layer 124 is made of dual layer of the BPSG and the PETEOS, the thickness of the BPSG may be about 5000Å and that of the PETEOS may be about 12000Å. At the cell array region A, the mold layer 124 and the second etch stopping layer 120 are sequentially patterned to form a storage node
5 hole 126 exposing the first pad contact plug 118a. A bottom electrode layer 128 is conformally stacked along a profile of the storage node hole 126, and a sacrificial layer 130 is stacked to fill the storage node hole 126. The bottom electrode layer 128 may be formed of titanium nitride with a thickness of 300Å by a CVD method. The sacrificial layer 130 may be
10 formed of hydrogen silsesquioxane (HSQ) or undoped silicate glass (USG).

Referring to Fig. 9, a planarization process is performed with respect to the sacrificial layer 130 and the bottom electrode layer 128 to remove the sacrificial layer 130 and the bottom electrode layer 126 on the mold layer 124. Therefore, the mold layer 124 is exposed and simultaneously, a bottom
15 electrode 128a and a sacrificial pattern (not illustrated) are formed in the storage node hole 126. The sacrificial pattern is removed by a wet etch process. The mold layer 124 is removed by a wet etch process to complete the bottom electrode 128a having a cylinder shape and electrically connecting to the first pad contact plug 118a. The mold layer 124 may be
20 removed by using a solution containing NH_4F and deionized water. A dielectric layer 130 and an upper electrode layer 132 are conformally stacked along a profile of the bottom electrode 128. The dielectric layer 130 may be preferably formed of hafnium oxide (HfO_M). The upper electrode

layer 132 may be preferably formed of titanium nitride with a thickness of about 400Å. Although not illustrated, a capping layer may be formed of tungsten with a thickness of about 1000Å on the upper electrode layer 132 in order to protect the upper electrode layer 132. At the peripheral circuit
5 region B, at least the upper electrode layer 132 is removed by a patterning process. Therefore, a capacitor composed of the bottom electrode 128a, the dielectric layer 130 and the upper electrode 132 is completed at the cell array region A.

Referring to Fig. 10, a second interlayer dielectric 134 is stacked to
10 cover the capacitor and the second etch stopping layer 120. The second interlayer dielectric 134 may be formed of a silicon oxide such as HDP with a thickness of about 26000Å. The second interlayer dielectric 134 and the second etch stopping layer 120 are patterned to form a metal contact hole 136 exposing the second pad contact plug 118b at the peripheral circuit
15 region B.

In a subsequent process, a second adhesion layer 138 is formed to cover inner sidewalls of the metal contact hole 136 by referring to Fig. 2, and a third conductive layer fills the metal contact hole 136 to form a metal contact plug 140. At this time, the second adhesion layer 138 may be formed
20 by a metal organic chemical vapor deposition (MOCVD) or an atomic layer deposition (ALD). When the second adhesion layer 138 is formed by the MOCVD method, the process temperature is preferably 300~400°C. If the second adhesion layer 138 is formed by the ALD method, the process

temperature is preferably 450~550°C.

[Effect of the Invention]

Therefore, according to the semiconductor device and the method of
5 forming the semiconductor device of the present invention, since an ohmic
layer is formed at a temperature higher than 600°C before forming a
capacitor, it is possible to prevent leakage current of the capacitor that may
occur at the high temperature. Additionally, since the resistor at the
peripheral circuit region and the buried contact plug at the cell array region
10 are made of the same material, it is possible to simplify the total process.

[Scope of the Claim]

[Claim 1]

5 A semiconductor device comprising:

 a semiconductor substrate having a cell array region and a peripheral circuit region;

 a lower interlayer dielectric covering the semiconductor substrate;

 a buried contact plug electrically connecting to the semiconductor
10 substrate through the lower interlayer dielectric at the cell array region;

 a resistor on the lower at the peripheral circuit region;

 a first interlayer dielectric covering the buried contact plug, the resistor, the lower interlayer dielectric;

 a first pad contact plug electrically connecting to the buried contact
15 plug through the first interlayer dielectric at the cell array region;

 a second pad contact plug electrically connecting to the resistor through the first interlayer dielectric at the peripheral circuit region;

 an ohmic layer interposed between the first pad contact plug and the buried contact plug and between the second pad contact plug and the

20 resistor;

 a capacitor having an upper electrode, a dielectric layer, and a bottom electrode electrically connecting to the first pad contact plug at the cell array region;

a second interlayer dielectric covering the capacitor and the first interlayer dielectric; and

a metal contact plug electrically connecting to the second pad contact plug through the first interlayer dielectric at the peripheral circuit region.

5

[Claim 2]

The semiconductor device as claimed in Claim 1, wherein the buried contact plug and the resistor are made of the same material.

10 [Claim 3]

The semiconductor device as claimed in Claim 2, wherein the same material is a doped polysilicon.

[Claim 4]

15 The semiconductor device as claimed in Claim 1, further comprising an etch stopping layer interposed between the first interlayer dielectric and the second interlayer dielectric.

[Claim 5]

20 The semiconductor device as claimed in Claim 1, wherein the ohmic layer is made of one selected from the group consisting of titanium silicide (TiSi_x), tantalum silicide (TaSi_y), cobalt silicide (CoSi_z) and nickel silicide (NiSi_w).

[Claim 6]

The semiconductor device as claimed in Claim 1, further comprising:

a first adhesion layer interposed between the first pad contact plug
and the first interlayer dielectric, between the first pad contact plug and the
5 buried contact plug, between the second pad contact plug and the first
interlayer dielectric, and between the second pad contact plug and the
resistor; and

a second adhesion layer interposed between the metal contact plug
and the first interlayer dielectric and between the metal contact plug and the
10 pad contact plug.

[Claim 7]

The semiconductor device as claimed in Claim 6, wherein the first
adhesion layer and the second adhesion layer are made of titanium nitride.

15

[Claim 8]

The semiconductor device as claimed in Claim 1, wherein the first
pad contact plug, the second pad contact plug and the metal contact plug are
made of one selected from the group consisting of tungsten, aluminum, and
20 copper.

[Claim 9]

A method of forming a semiconductor device comprising:

defining a cell array region and a peripheral circuit region at a semiconductor substrate;

stacking a lower interlayer dielectric at the semiconductor substrate;

forming a contact hole exposing the semiconductor substrate at the
5 cell array region by patterning the lower interlayer dielectric;

filling the contact hole by stacking a first conductive layer at an entire surface of the semiconductor substrate having the contact hole;

patterning the first conductive layer to form a buried contact plug
filling the contact hole at the cell array region and simultaneously to form a
10 resistor on the lower interlayer dielectric at the peripheral circuit region;

forming a first interlayer dielectric to cover the semiconductor substrate having the buried contact plug and the resistor;

patterning the first interlayer dielectric to form a first pad contact hole exposing the buried contact plug and simultaneously to form a second
15 pad contact hole exposing a part of the resistor;

forming an ohmic layer to cover at least bottoms of the first pad contact hole and the second pad contact hole;

filling the first pad contact hole and the second pad contact hole by stacking a second conductive layer;

20 planarizing the second conductive layer to expose the first interlayer dielectric and to form a first pad contact plug in the first pad contact hole and a second pad contact plug in the second pad contact hole;

forming an etch stopping layer to cover the first pad contact plug, the

second pad contact plug and the first interlayer dielectric;

forming a capacitor having an upper electrode, a dielectric layer and a bottom electrode electrically connecting to the first pad contact plug through the etch stopping layer;

5 forming a second interlayer dielectric at an entire surface of the semiconductor substrate;

forming a metal contact hole exposing the second pad contact plug by patterning the second interlayer dielectric at the peripheral circuit region; and

10 forming a metal contact plug by filling the metal contact hole with a third conductive layer.

[Claim 10]

The method as claimed in Claim 9, further comprising forming an
15 etch stopping layer before forming the second interlayer dielectric.

[Claim 11]

The method as claimed in Claim 9, wherein the first conductive layer is made of a doped polysilicon.

20

[Claim 12]

The method as claimed in Claim 9, wherein the forming of an ohmic layer comprises:

forming a metal layer covering at least bottoms of the first pad
contact hole and the second pad contact hole;

performing a rapid thermal process with respect to the metal layer to
form an ohmic layer at boundaries between the metal layer and the buried
5 contact plug and between the metal layer and the resistor.

[Claim 13]

The method as claimed in Claim 12, wherein the rapid thermal
process is performed at a temperature of about 600~900°C for about 10~30
10 seconds.

[Claim 14]

The method as claimed in Claim 9, wherein the ohmic layer is made
of one selected from the group consisting of titanium silicide (TiSi_x),
15 tantalum silicide (TaSi_y), cobalt silicide (CoSi_z) and nickel silicide (NiSi_w).

[Claim 15]

The method as claimed in Claim 9, further comprising:

forming a first adhesion layer to cover sidewalls and bottoms of the
20 first pad contact hole and the second pad contact hole before forming the
second conductive layer; and

forming a second adhesion layer to cover sidewalls and a bottom of
the metal contact hole before forming the third conductive layer.

[Claim 16]

The method as claimed in Claim 15, wherein the first adhesion layer and the second adhesion layer are made of titanium nitride.

5 [Claim 17]

The method as claimed in Claim 9, wherein the second conductive layer and the third conductive layer are made of one selected from the group consisting of tungsten, aluminum, and copper.

10 [Claim 18]

The method as claimed in Claim 9, wherein the forming a capacitor comprises:

forming a mold layer on the etch stopping layer;

15 sequentially patterning the mold layer and the etch stopping layer at the cell array region to form a storage node hole exposing the first pad contact plug;

conformally forming a bottom electrode layer at an entire surface of the semiconductor substrate having the storage node hole;

20 filling the storage node hole by stacking a sacrificial layer on the bottom electrode layer;

removing the bottom electrode layer and the sacrificial layer on the mold layer by a planarization process to form a bottom electrode and a sacrificial pattern in the storage node hole;

removing the sacrificial pattern and the mold layer to leave the bottom electrode;

conformally stacking a dielectric layer and an upper electrode layer on the semiconductor substrate having the bottom electrode; and

5 removing at least the upper electrode layer at the peripheral circuit region.

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